contact, diode D_3, and the limit switch, LS−. You need the diode to avoid feeding voltage to the −Limit input through the activated LS+ limit switch. The motor now runs in the opposite direction until the limit switch LS− activates. At that instant, the driver is disabled (for the negative direction), and relay K_1 turns off. The cycle begins anew.

The values of the components the circuit uses depend principally on the selected servoamplifier and motor, thus **Figure 1** shows no values. The machine has worked satisfactorily in two shifts for more than two years. During this period, contrary to our expectations, we never readjusted the servoamplifier.

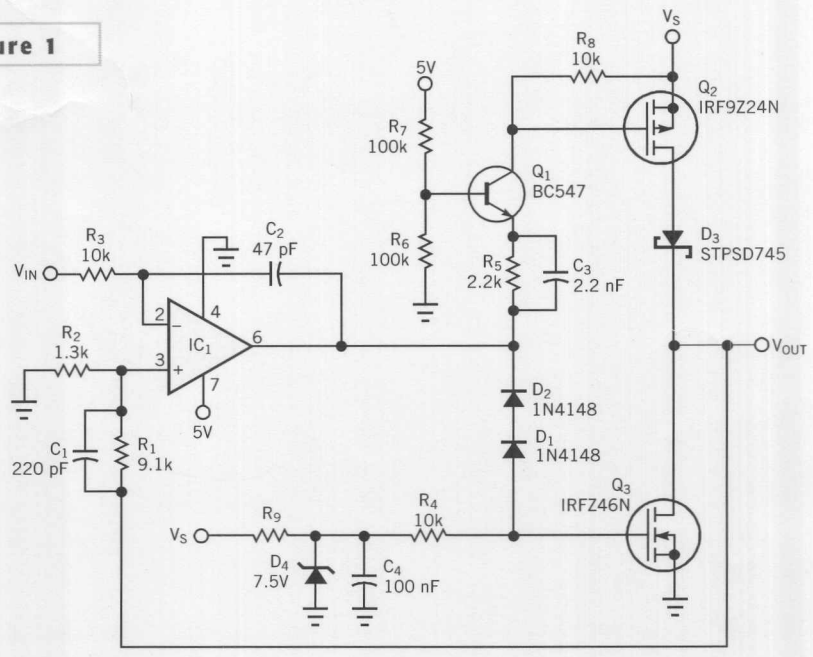
Is this the best Design Idea in this issue? Select at www.edn.com.

Linear power driver works from single supply

Tom Gay, Darmstadt, Germany

In low-power, single-supply analog applications, it is often desirable to maintain precise control of voltages much greater than the positive-supply rail. The circuit in **Figure 1** allows you to amplify the input voltage, V_{IN}, by a factor, A, which resistors R_1 and R_2 set. The output voltage, V_{OUT}, equals AV_{IN}, where $A=R_2/(R_1+R_2)$. The op amp receives its supply from a single 5V source, and the discrete output stage operates from a rectified voltage, V_S, from a power source that meets the requirements of the application. When the circuit neither sinks nor sources current, the op amp's output settles to a voltage higher than 1.9V (Q_1 is completely off) but lower than the threshold voltage of the n-channel FET, Q_3, minus 1.2V (two diode drops). When V_{IN} rises from a given state, the op amp's output voltage drops and gradually turns on Q_1. This action results in a voltage drop across R_8, turning on Q_2. This process continues until the voltages at the op amp's two inputs match. A decreasing V_{IN} causes the op amp's output voltage to rise to the point at which Q_3 conducts enough to pull down V_{OUT}. Capacitors C_1, C_2, and C_3 are necessary to prevent oscillation.

Figure 1



This simple circuit allows you to control voltages far in excess of the positive-supply rail.

The circuit, useful as a power driver for pulse generators, offers rise and fall times of less than 15 µsec, virtually independently of the supply voltage, V_S. You can test the design with op amps LMC7101, LT1013, and AD8551. All these op amps deliver load currents as high as 5A at voltages as high as $V_S=40V$. One important feature of the design is its insensitivity to component tolerances. The values for R_1 and R_2 in **Figure 1** yield A=8. The value of R_9 depends on V_S. You could use a logic-level FET, such as the IRLZ34N for Q_3; you can then omit the components D_1, D_2, D_4, R_4, R_9, and C_4. In this case, the op amp's output connects directly to the gate of Q_3, and you must reduce the value of R_6 to lower the base voltage of Q_1 to maintain the "idle window" in which both Q_1 and Q_3 are off. The op amp's input-voltage range must include ground. D_3 is necessary only in cases in which sources connect to the output. D_3 prevents reverse current flow from the external source through Q_2. Such a situation can arise when the circuit serves in a battery-charger application.

Is this the best Design Idea in this issue? Select at www.edn.com.